



XFT Finder Upgrade

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Proposal:

- To build next version of XFT Finder Board using optical input cables.
- A single version of the board should be capable of performing the function of a Stereo Finder, a SL1/3 Finder and a SL2/4 Finder.



TDC Data

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TDC data:

- Each TDC has 96 channels of wire data. Currently, two Ansley cables are used to carry the prompt/delay information up the cables every 132ns.
- The new design would replace each Ansley cable with an optical data link.
- The link would carry at least 6 time slices of information from 48 channels (half a TDC) every 396ns.



Optical Data Link

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Data link:

- Assume we use a serializer such as the TI TLK1501. This serializer has 8b/10b encoding and can go up to 1.5Gbps. A possible data format would be the following:



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Word #	TX_EN	TX_ER	Data
1	0	1	Carrier extend(K23.7, K23.7) indicates start of new data block
2	1	0	Bit 0 represents Beam Zero
3	1	0	Wires 0-15 time slice 0
4	1	0	Wires 16-32 time slice 0
5	1	0	Wires 32-47 time slice 0
6	1	0	Wires 0-15 time slice 1
7	1	0	Wires 16-32 time slice 1
8	1	0	Wires 32-47 time slice 1
9	1	0	Wires 0-15 time slice 2
10	1	0	Wires 16-32 time slice 2
11	1	0	Wires 32-47 time slice 2
12	1	0	Wires 0-15 time slice 3
13	1	0	Wires 16-32 time slice 3
14	1	0	Wires 32-47 time slice 3
15	1	0	Wires 0-15 time slice 4
16	1	0	Wires 16-32 time slice 4
17	1	0	Wires 32-47 time slice 4
18	1	0	Wires 0-15 time slice 5
19	1	0	Wires 16-32 time slice 5
20	1	0	Wires 32-47 time slice 5



Rates and Clocking

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- Assume we also want to add in one or two “Idle” patterns to maintain link synchronization – this gives us about 22 words to send in 396ns. This works out to a link rate of
- This gives us a clocking frequency of about 55.6Mhz for the link.
- These links expect a very low clock jitter (40ps or less). It would be advisable to run the serializers off their own local oscillators.

FPGA logic would need to take care of syncing from and back to the CDF_Clock.



Neighbor sharing – Option A

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The optical input cables go directly into the main board. This means we would not use the backplane to share neighbor information. We would therefore have to drive copies of all wires which are neighbors to adjacent boards.

- **Maximum number of Optical input cables:**

SL1/3 board: SL1-N, SL1-A, SL1-B, SL1+N, SL3-N, SL3-A, SL3-B, SL3-C, SL3-D, SL3+N (10 inputs)

SL2/4 board: SL2-N, SL2-A, SL2-B, SL2-C, SL2+N, SL4-N, SL4-A, SL4-B, SL4-C, SL4-D, SL4-E, SL4+N (12 inputs)

Stereo: ??

- **Current 360 Ansley cables -> 528 Optical Links**



Neighbor sharing – Option B

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The optical input cables go to a transition module. This means we keep the backplane to share neighbor information.

- **Current 360 Ansley cables -> 360 Optical Links**



O/E and E/O Examples

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M2R-25-4-1-TL Optical Gigabit Ethernet/Fibre Channel
850nm SFF 2x5 Dual Receivers -- 1.25/1.0625GBaud --- +3.3V



Dual Receivers



Features

- 1.25 Gbps Gigabit Ethernet Compliant
- Metalized Plastic Package
- TTL Signal Detect output
- AC coupled PECL level outputs
- Low profile fits Mezzanine Card Applications
- Single +3.3V Power Supply
- Wave Solderable / Aqueous Washable
- Class 1 Laser Safety Compliant
- UL 1950 Approved

PRODUCT OVERVIEW

The M2R-25-4-1-TL Small Form Factor (SFF) optical dual receiver modules are high performance integrated duplex data links for uni-directional communication over multimode optical fibre. The M2R-25-4 module is

M2T-25-4-1-L Optical Gigabit Ethernet/Fibre Channel
850nm SFF LC 2x5 Dual Transmitters - 1.25/1.0625GBaud -- +3.3V



Dual Transmitters



Features

- 1.25 Gbps Gigabit Ethernet Compliant
- 1.0625Gbps Fibre Channel Compliant
- Metalized Plastic Package
- AC coupled PECL level inputs
- Low profile fits Mezzanine Card Applications
- Single +3.3V Power Supply
- Wave Solderable / Aqueous Washable
- Class 1 Laser Safety Compliant
- UL 1950 Approved

PRODUCT OVERVIEW

The M2T-25-4-1-L Small Form Factor (SFF) optical dual transmitter modules are high performance integrated duplex data links for uni-directional communication over multimode optical fibre. The M2T-25-4 module is specifically designed to be used in Gigabit Ethernet/ Fibre



Serializer/De-Serializer

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TLK1501 0.6 TO 1.5 GBPS TRANSCEIVER

SLLS428F – JUNE 2000 – REVISED JANUARY 2004

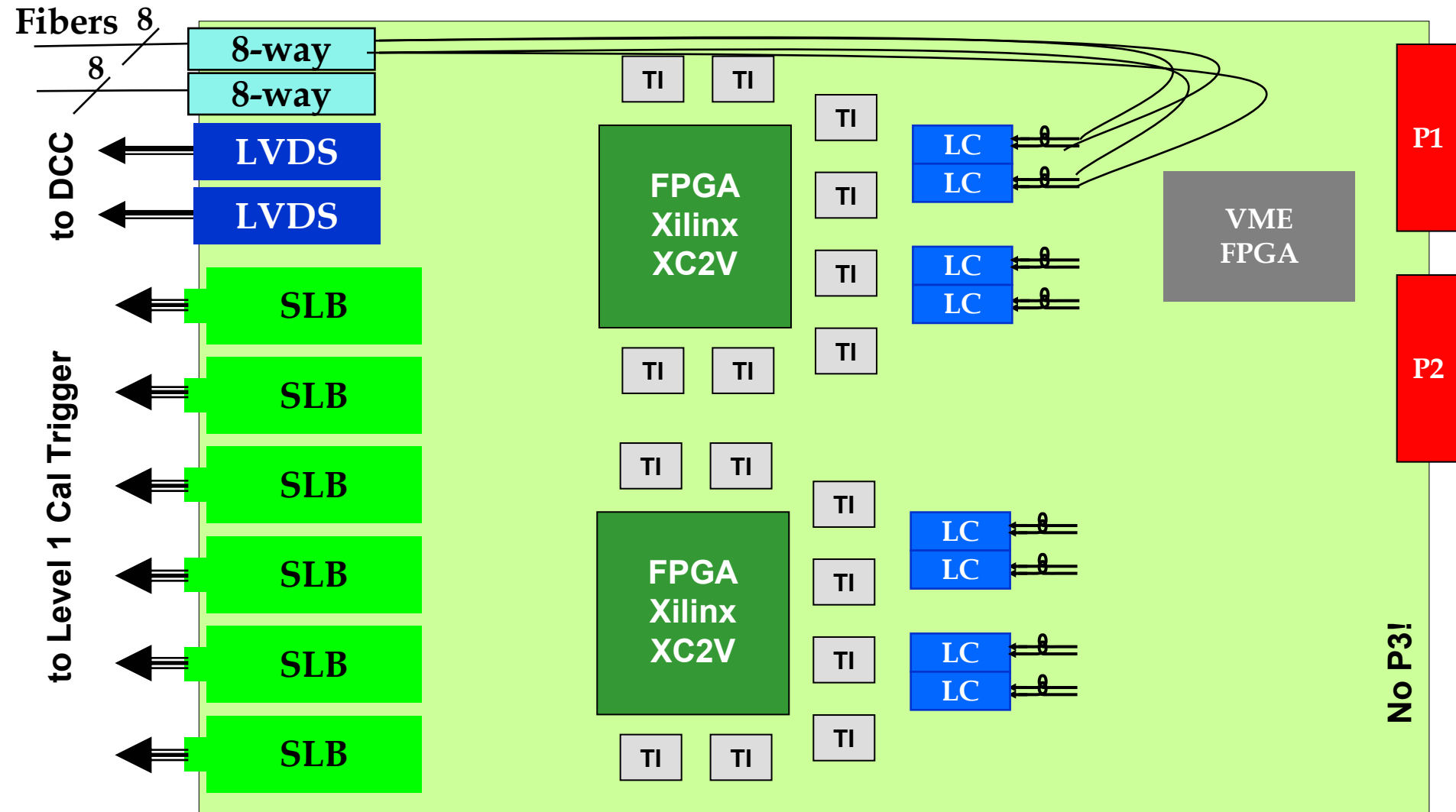
- Hot Plug Protection
- 0.6 to 1.5 Gigabits Per Second (Gbps) Serializer/Deserializer
- High-Performance 64-Pin VQFP Thermally Enhanced Package (PowerPAD™)
- 2.5 V Power Supply for Low Power Operation
- Programmable Voltage Output Swing on Serial Output
- Interfaces to Backplane, Copper Cables, or Optical Converters
- Rated for Industrial Temperature Range
- On-Chip 8-Bit/10-Bit (8B/10B) Encoding/Decoding, Comma Alignment, and Link Synchronization
- On-Chip PLL Provides Clock Synthesis From Low-Speed Reference
- Receiver Differential Input Thresholds 200 mV Minimum
- Typical Power: 250 mW
- Loss of Signal (LOS) Detection
- Ideal for High-Speed Backplane Interconnect and Point-to-Point Data Link



Example of similar board used for CMS HCA

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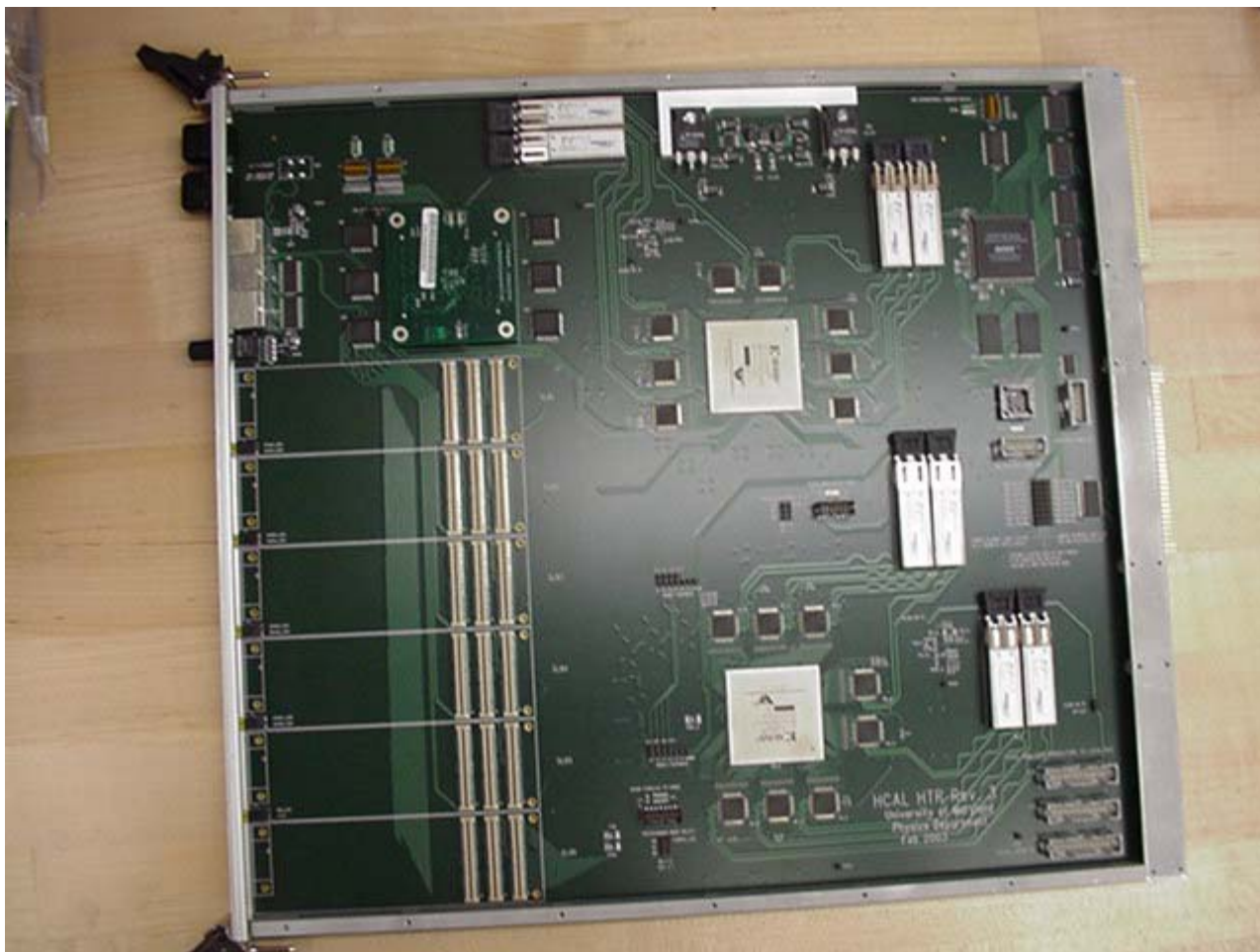
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Picture of HCAL HTR

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Main Module does it all

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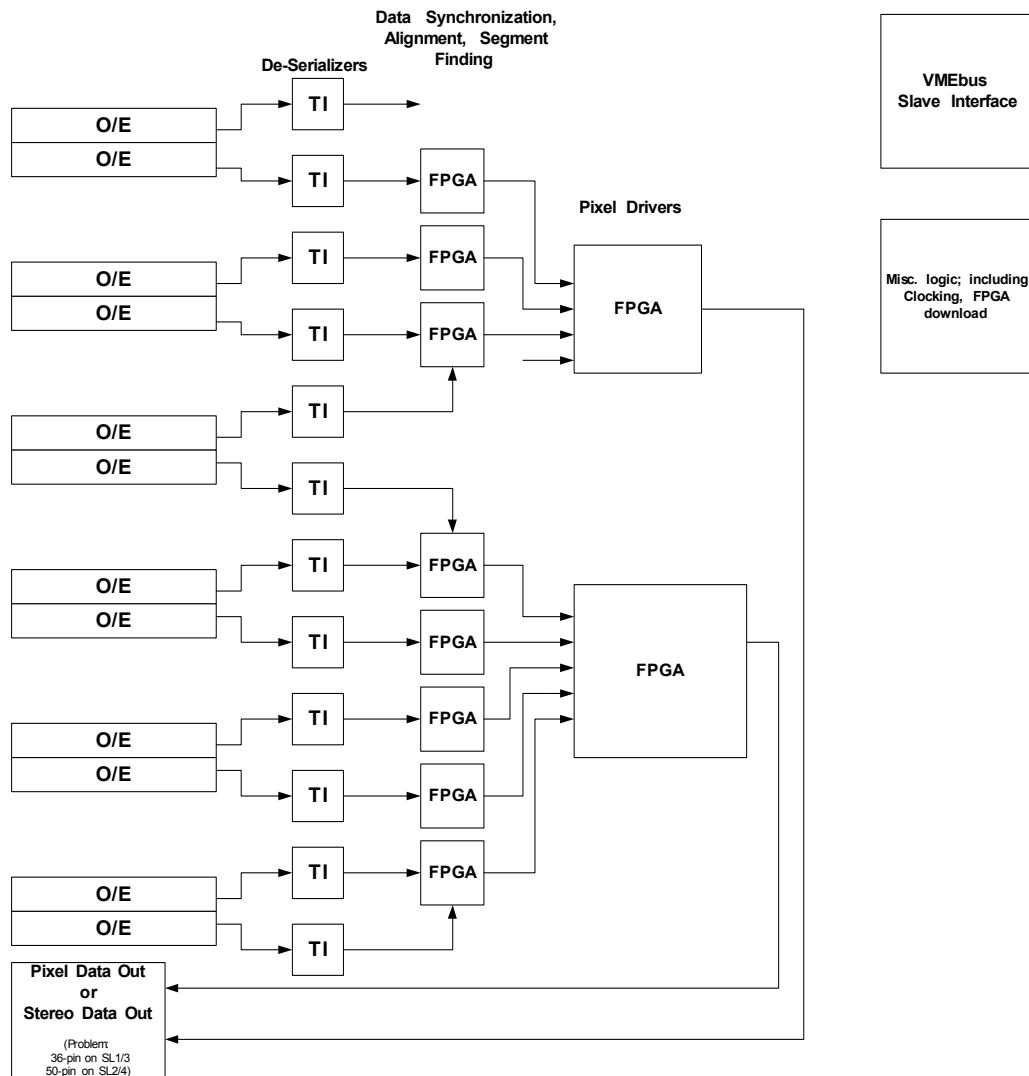
Single Board Option (no transition module)

- 6 dual O/E parts on front panel
- 2 Pixel driving connectors on front panel
(Note: SL1/3 modules use 36 pin connectors, SL2/4 modules use 50 pin connectors)
- 12 TI TLK1501 Serializers/De-serializers
- 8 “Finder” FPGAs
 - receive data
 - re-synchronize to CDF_Clock
 - Align data across links
 - Feed neighbor information to adjacent chips
 - Segment Finding
- 1 or 2 “Pixel” FPGA(s)
- 1 “Stereo Output” FPGA and PCI driver
- 1 VME slave FPGA
- Download/control logic



Single Board Option

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Main/Transition Modules

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Transition module

- 4 dual O/E parts on front panel
- 8 TI TLK1501 Serializers/De-serializers
- 1-2 FPGAs
 - receive data
 - re-synchronize to CDF_Clock
 - Align data across links

Backplane

- Re-use current backplane for neighbor sharing

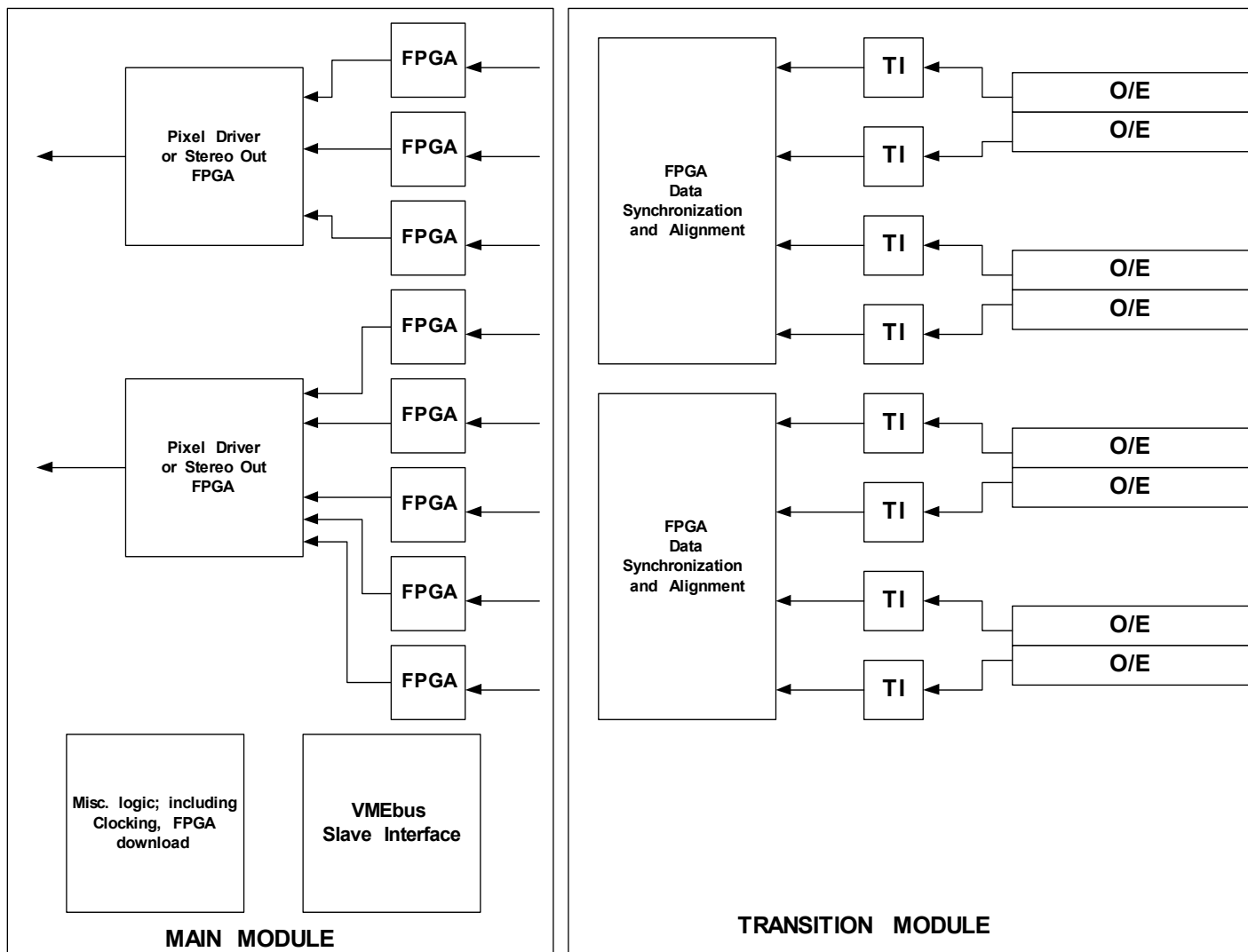
Main Module

- 8 “Finder” FPGAs
 - Segment Finding
- 2 Pixel driving connectors on front panel
(Note: SL1/3 modules use 36 pin connectors, SL2/4 modules use 50 pin connectors)
- 1 “Stereo Output” FPGA and PCI driver
- 1 VME slave FPGA
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Main/Transition Module Solution

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Which Option?

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Main/transition Module

- Pros

- Fewer expensive optical links (528 vs 360)

- Optical links protected in rear of crate

- Can start transition module design/layout right away!

- Cons

- Need to build ~60 transition cards

- Data is all fanned in through P3/4 backplane connectors

Is there any benefit to making these backward compatible with present XFT Finders?

I suspect cost and effort is a wash between the two options.



What do we need now?

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Need feedback on what size segment finding FPGA is needed?

- Stick with Altera to make transition from old mask sets easier?
- Size dependent on studies of mask sets.

Do we pursue single board option or main/transition module solution?